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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/158,616	09/22/98	DALAL H	P19-98-065

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EXAMINER
FOSTER,D

ART UNIT	PAPER NUMBER
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/158,616	Applicant(s) Dalal et al.
	Examiner David Foster	Group Art Unit 2841

☒ Responsive to communication(s) filed on *Sep 22, 1998*.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-52* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☒ Claim(s) *20-52* is/are allowed.

☒ Claim(s) *1-3, 5-7, 9, 12-14, 16, and 17* is/are rejected.

☒ Claim(s) *4, 8, 10, 11, 15, 18, and 19* is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *2*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

A MULTI-LEVEL ELECTRONIC PACKAGE

AND METHOD FOR MAKING SAME

Dalal et al.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5-7, 9, 12-14 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marcantonio (5,796,170). **Reference claim** 1.Marcantonio discloses package for containing electronic components, the package comprising: a first circuitized card (Figure 4, item 224, 226 and 228); a second circuitized card (Figure 4, item 138); an interposer interposed between the first and second circuitized cards (Figure 8), the interposer having an opening (Figure 8), the opening of the interposer and the first and second circuitized card forming a cavity for containing at least one electronic component. **Reference claim** 2. The package of claim 1 wherein the interposer, first circuitized card and second circuitized card act as a Faraday shield for electronic components placed inside the cavity (column 5, line 26). **Reference claim** 3. The

package of claim 2 wherein the interposer has at least one connection to at least one ground (column 5, line 26). **Reference claim** 5. The package of claim 1 wherein the opening is square and is in the approximate center of the interposer (Figure 8). **Reference claim** 6. The package of claim 1 wherein the interposer is electrically and physically connected to the first and second circuitized cards (Figure 4). **Reference claim** 7. The package of claim 1 wherein the first circuitized card has a top surface and there is at least one component mounted to the top surface (Figure 4). **Reference claim** 9. The package of claim 1 wherein the second circuitized card has a top surface and there is at least one component mounted to the top surface (Figure 4). **Reference claim** 12. The package of claim 1 wherein the second circuitized card has a bottom surface and the bottom surface has a ball grid array allowing connection to a system board (Figure 4). **Reference claim** 13. The package of claim 6 wherein the first circuitized card and interposer are connected through surface mount or through-hole technologies and wherein the interposer and the second circuitized card are connected through surface mount or through-hole technologies (Figure 4, items 242). **Reference claim** 14. The package of claim 13 wherein the interposer and first circuitized card are connected through a ball grid array and the interposer and the second circuitized card are connected through a ball grid array (Figure 4). **Reference claim** 16. The package of claim 1 wherein at least one component is mounted to the first circuitized card and wherein the at least one component is attached to a heat sink or pick-up plate (Figure 4, item 14). **Reference claim** 17. The package of claim 1 wherein the cavity contains at least one component (Figure 4, item 212).

Allowable Subject Matter

3. Claims 4, 8, 10, 11, 15, 18 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 20-35 and 36-52 are allowed.

5. The following is an examiner's statement of reasons for allowance: Cited prior art does not teach nor disclose a package comprising electronic components and having first and second circuitized cards, an interposer electrically connecting the circuitized cards, top and bottom circuit cards having at least one electronic component as well as an opening in the interposer, the bottom surface of the first circuitized card and the top surface of the second circuitized care for a cavity for containing at least one electronic component.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The best art to consider with this application can be found in Beaman et al. (5,371,654), Grabbe et al. (4,699,593), Dranchak et al. (5,953,214), Booth et al. (5,384,955), Iwasaki (5,834,848), Buckley, III et al. (5,477,082), Kim (5,978,229), Bertin et al. (5,977,640),

Pasch (5,468,681), Beilin et al. (5,854,534), Chan (5,838,551) and Higgins, III (5,639,989). Beaman et al. disclose a structure having two subcomponent assemblies each with a substrate and a multilevel wiring structure, Grabbe et al. disclose a chip carrier having a housing frame, contact modules and contact pads on a substrate, Dranhchak et al. disclose a dual substrate package having an intermediate connection between the substrates, Booth et al. disclose a method of replacing IC ship package wiring having an interposing, Iwasaki et al. disclose an electronic device and semiconductor package mounted on a motherboard and a buffer layer for relieving a stress, Buckley, III et al. disclose a bi-planar multi-chip module which has a die mounted on both sides of an insulating flexible carrier, Kim discloses an apparatus and a process for mounting integrated circuit packages on circuit boards, Bertin et al. disclose a chip-on-chip component connection/interconnection for electrically connecting the fully functional chips to external circuitry, Pasch discloses a process for interconnecting conductive substrates using an interposer having conductive plastic filled vias, Beilin et al. disclose an interposer substrate for mounting an integrated circuit chip to a substrate, Chan discloses an electronic package with an electronic component mounted on a PCB or ceramic substrate wherein the component is protected by an EMI shield and Higgins, III discloses electronic components shield from electromagnetic interference (EMI) by one or more conformal layers filled with selected filler particulars for attenuating specific EMI frequencies.

Any inquiry concerning to this communication or earlier communications from the Examiner should be directed to David Foster whose telephone number is (703) 308-1763. The examiner can normally be reached on Monday through Thursday and alternate Fridays.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Jeffrey A. Gaffin, who can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703)308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

DAF

July 29, 2000

Jeffrey Gaffin
Supervisory Patent Examiner
Technology Center 2800